ABSTRACT

A semiconductor device (700) having a leadframe with a first plurality of segments (110) having a narrow end portion (111) in a first horizontal plane (211) and a wide end portion (112) in a second horizontal plane (212). The leadframe further includes a second plurality of segments (120) having a narrow center portion (121) in the first horizontal plane, at least one wide center portion (122) in the second horizontal plane, and narrow end portions (123) in a third horizontal plane (213), which is located between the first and second planes. The wide segment portions may be covered by a layer of noble metal or by a layer of solderable metal. The narrow end portions of the first segment plurality and the narrow central portions of the second segment plurality may be covered by a layer of noble metal or a layer of solderable metal. An integrated circuit chip (601) has on its active surface a first plurality of contact pads (703) located in the peripheral chip portions, and a second plurality of contact pads (704) centrally located, each pad with an interconnection element. The narrow end portions of the first plurality of leadframe segments are attached to the interconnection elements on the first plurality of chip contact pads, respectively. The narrow central portions of the second plurality of leadframe segments are attached to the interconnection elements on the second plurality of chip contact pads, respectively. The device is protected by an encapsulation material (730), leaving the external segment surfaces (712a, 722a) in the second plane (212) exposed.